REMARKS

Applicants respectfully request reconsideration of this application. Claims 1-26 are pending. Claims 1-7, 10-14, 16-22, 24, and 26 have been amended to more properly define preexisting claim limitations and are supported by the specification.

In the Office Action, the Abstract is objected to for minor informalities. Applicants have amended the Abstract to overcome the objection. The Examiner is respectfully requested to withdraw the objection.

The Examiner objected to the claims for minor informalities. Accordingly, Applicants have amended claims 1-7, 10-14, 16-22, 24, and 26 to overcome the objection. Withdrawal of the objection is respectfully requested.

Applicants have amended the claims, particularly to overcome the Examiner's rejection of indefiniteness under 35 U.S.C. §112 and to more clearly distinguish the invention from the prior art cited. The Examiner initially rejected claims 1-29 under 35 U.S.C. §112, second paragraph. Accordingly, Applicant has amended claims 1-7, 10-14, 16-22, 24, and 26 to particularly point out and distinctly claim, in full, clear, concise and exact terms, the subject matter which Applicant regards as his invention.

In the Office Action, Examiner rejected claims 1-26 under 35 U.S.C. §102(b) for being anticipated by any one of Caceres et al. (U.S. 5,802,554; hereinafter, "Caceres"), Bains et al. (U.S. 5,678,009; hereinafter, "Bains"), or Marisetty (U.S. 5,666,521; hereinafter, "Marisetty"). Applicants respectfully traverse the rejection.

Claim 1 as amended sets forth a logic unit to generate a command occurrence signal to identify when a command signal is issued, wherein a plurality of data transfer operations on one of the one or more memory devices are completed in response to the command occurrence signal, a transition of a flag signal, and a chip select signal

corresponding to the one memory device. In contrast, none of the cited references discloses at least the above limitation.

According to Caceres, the system disclosed includes a memory management unit (MMU) 420 that manages the main memory and/or the flash memory by tracking addresses in the corresponding memory (Caceres, Figure 4; col. 4, lines 13-67). However, Caceres merely discloses that the MMU 420 "controls many of the control input signals (not shown) for each of the memories such as chip enable, read/write, chip select, etc." (Caceres, col. 4, lines 50-54). Caceres fails to disclose at least the logic unit set forth in claim 1. Therefore, Caceres does not anticipate claim 1. Withdrawal of the rejection is respectfully requested.

Regarding Bains, it discloses a timing circuit 27 in a graphics controller 26 to determine when the graphics controller 26 can assume control of the memory bus (Bains, col. 6, lines 31-39; Figure 3). Therefore, Bains does not disclose a logic unit to generate a command occurrence signal. Bains does not anticipate claim 1 for at least this reason. Withdrawal of the rejection is respectfully requested.

Finally, Marisetty discloses a system for performing data transfer between two memories sharing common data and address busses. Marisetty discloses strobing column and row addresses to manage data transfers to/from the two memories (Marisetty, col. 3, lines 26-42). Marisetty does not disclose a logic unit to generate a command occurrence signal. Therefore, Marisetty does not anticipate claim 1 for at least this reason. Withdrawal of the rejection is respectfully requested.

For at least the reason discussed above with respect to claim 1, claims 7, 17, and 22 are not anticipated by any one of Caceres, Bains, and Marisetty. Applicants respectfully request withdrawal of the rejection.

Claims 2-6, 8-16, 18-21, and 23-26 depend, directly or indirectly, from claims 1, 7, 17, and 22. Therefore, none of Caceres, Bains, and Marisetty anticipates claims 2-6, 8-

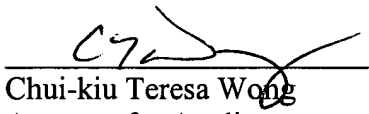
16, 18-21, and 23-26 for at least the reason discussed above with respect to claim 1. Applicants respectfully request the Examiner to withdraw the rejections.

Accordingly, Applicant respectfully submits that the objections and the rejections under 35 U.S.C. §112, second paragraph, and §102(b) have been overcome by the amendments and the remarks and withdrawal of these rejections is respectfully requested. Applicant submits that claims 1-7, 12, and 20-29 as amended are now in condition for allowance and such action is earnestly solicited.

If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: June 18, 2004



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